4.1.1.1 GWT Package

4.1.1.1.1 Multi-Buffered Analog-to-Digital Converters (MibADC)

Table 4-1. GWT Multi-Buffered Analog-to-Digital Converters (MibADC1, MibADC2)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
ADREFHI(1)	V15	Input	-	None	ADC high reference supply
ADREFLO(1)	V16	Input			ADC low reference supply
VCCAD(1)	W15	Power			Operating supply for ADC
VSSAD	V19	Ground	-	None	ADC supply power
	W16				
	W18				
	W19				
AD1EVT	N19	I/O	Pull Down	Programmable, 20uA	ADC1 event trigger input, or GPIO
MIBSPI3NCS[0]/**AD2EVT**/GIOB[2]/N2HET2_PIN_nDIS	V10	I/O	Pull Up	Programmable, 20uA	ADC2 event trigger input, or GPIO
AD1IN[0]	W14	Input	-	None	ADC1 analog input
AD1IN[1]	V17				
AD1IN[2]	V18				
AD1IN[3]	T17				
AD1IN[4]	U18				
AD1IN[5]	R17				
AD1IN[6]	T19				
AD1IN[7]	V14				
AD1IN[8] / AD2IN[8]	P18	Input	-	None	ADC1/ADC2 shared analog inputs
AD1IN[9] / AD2IN[9]	W17				
AD1IN[10] / AD2IN[10]	U17				
AD1IN[11] / AD2IN[11]	U19				
AD1IN[12] / AD2IN[12]	T16				
AD1IN[13] / AD2IN[13]	T18				
AD1IN[14] / AD2IN[14]	R18				
AD1IN[15] / AD2IN[15]	P19				
AD1IN[16] / AD2IN[0]	V13				
AD1IN[17] / AD2IN[1]	U13				
AD1IN[18] / AD2IN[2]	U14				
AD1IN[19] / AD2IN[3]	U16				
AD1IN[20] / AD2IN[4]	U15				
AD1IN[21] / AD2IN[5]	T15				
AD1IN[22] / AD2IN[6]	R19				
AD1IN[23] / AD2IN[7]	R16				

(1) The ADREFHI, ADREFLO, VCCAD and VSSAD connections are common for both ADC cores.

4.1.1.1.2 Enhanced High-End Timer Modules (N2HET)

Table 4-2. GWT Enhanced High-End Timer Modules (N2HET)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
N2HET1[0]/SPI4CLK	K18	I/O	Pull Down	Programmable, 20uA	N2HET1 time input capture or output compare, or GIO. Each terminal has a suppression filter that ignores input pulses smaller than a programmable duration.
N2HET1[1]/SPI4NENA/N2HET2[8]	V2				
N2HET1[2]/SPI4SIMO[0]	W5				
N2HET1[3]/SPI4NCS[0]/N2HET2[10]	U1				
N2HET1[4]	B12				
N2HET1[5]/SPI4SOMI[0]/N2HET2[12]	V6				
N2HET1[6]/SCIRX	W3				
N2HET1[7]/N2HET2[14]	T1				
N2HET1[8]/MIBSPI1SIMO[1]	E18				
N2HET1[9]/N2HET2[16]	V7				
N2HET1[10]	D19				
N2HET1[11]/MIBSPI3NCS[4]/N2HET2[18]	E3				
N2HET1[12]	B4				
N2HET1[13]/SCITX	N2				
N2HET1[14]	A11				
N2HET1[15]/MIBSPI1NCS[4]	N1				
N2HET1[16]	A4				
N2HET1[17]	A13				
N2HET1[18]	J1				
N2HET1[19]	B13				
N2HET1[20]	P2				
N2HET1[21]	H4				
N2HET1[22]	B3				
N2HET1[23]	J4				
N2HET1[24]/MIBSPI1NCS[5]	P1				
N2HET1[25]	M3				
N2HET1[26]/	A14				
N2HET1[27]	A9				
N2HET1[28]/	K19				
N2HET1[29]	A3				
N2HET1[30]	B11				
N2HET1[31]	J17				
GIOA[5]/EXTCLKIN/**N2HET1_PIN_nDIS**	B5	I/O	Pull Down	Programmable, 20uA	

Table 4-2. GWT Enhanced High-End Timer Modules (N2HET) (continued)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
GIOA[2]/**N2HET2[0]**	C1	I/O	Pull Down	Programmable, 20uA	N2HET2 time input capture or output compare, or GIO. Each terminal has a suppression filter that ignores input pulses smaller than a programmable duration.
EMIF_ADDR[0]/**N2HET2[1]**	D4				
GIOA[3]/**N2HET2[2]**	E1				
EMIF_ADDR[1]/**N2HET2[3]**	D5				
GIOA[6]/**N2HET2[4]**	H3				
EMIF_BA[1]/**N2HET2[5]**	D16				
GIOA[7]/**N2HET2[6]**	M1				
EMIF_nCS[0]/RTP_DATA[15]/**N2HET2[7]**	N17				
N2HET1[1]/SPI4NENA/**N2HET2[8]**	V2				
EMIF_nCS[3]/RTP_DATA[14]/**N2HET2[9]**	K17				
N2HET1[3]/SPI4NCS[0]/**N2HET2[10]**	U1				
EMIF_ADDR[6]/RTP_DATA[13]/**N2HET2[11]**	C4				
N2HET1[5]/SPI4SOMI[0]/**N2HET2[12]**	V6				
EMIF_ADDR[7]/RTP_DATA[12]/**N2HET2[13]**	C5				
N2HET1[7]/**N2HET2[14]**	T1				
EMIF_ADDR[8]/RTP_DATA[11]/**N2HET2[15]**	C6				
N2HET1[9]/**N2HET2[16]**	V7				
N2HET1[11]/MIBSPI3NCS[4]/**N2HET2[18]**	E3				
MIBSPI3NCS[0]/AD2EVT/GIOB[2]/**N2HET2_PIN_nDIS**	V10	I/O	Pull Up	Programmable, 20uA	

4.1.1.1.3 General-Purpose Input / Output (GPIO)

Table 4-3. GWT General-Purpose Input / Output (GPIO)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
GIOA[0]	A5	I/O	Pull Down	Programmable, 20uA	General-purpose I/O. All GPIO terminals are capable of generating interrupts to the CPU on rising / falling / both edges.
GIOA[1]	C2				
GIOA[2]/N2HET2[0]	C1				
GIOA[3]/N2HET2[2]	E1				
GIOA[4]	A6				
GIOA[5]/EXTCLKIN/N2HET1_PIN_nDIS	B5				
GIOA[6]/N2HET2[4]	H3				
GIOA[7]/N2HET2[6]	M1				
GIOB[0]	M2				
GIOB[1]	K2				
GIOB[2]	F2				
GIOB[3]	W10				
GIOB[4]	G1				
GIOB[5]	G2				
GIOB[6]	J2				
GIOB[7]	F1				
MIBSPI3NCS[0]/AD2EVT/**GIOB[2]**/N2HET2_PIN_nDIS	V10		Pull Up	Fixed 20uA pull down	GIOB[2] is input only on this terminal. When GIOB[2] function is selected, the pull is a fixed pull down

4.1.1.1.4 FlexRay Interface Controller (FlexRay)

Table 4-4. FlexRay Interface Controller (FlexRay)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
FRAYRX1	A15	Input	Pull Up	Fixed, 100uA	FlexRay data receive (channel 1)
FRAYTX1	B15	Output	None	-	FlexRay data transmit (channel 1)
FRAYTXEN1	B16	Output			FlexRay transmit enable (channel 1)
FRAYRX2	A8	Input	Pull Up	Fixed, 100uA	FlexRay data receive (channel 2)
FRAYTX2	B8	Output	None	-	FlexRay data transmit (channel 2)
FRAYTXEN2	B9	Output			FlexRay transmit enable (channel 2)

4.1.1.1.5 Controller Area Network Controllers (DCAN)

Table 4-5. GWT Controller Area Network Controllers (DCAN)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
CAN1RX	B10	I/O	Pull Up	Programmable, 20uA	CAN1 receive, or GPIO
CAN1TX	A10				CAN1 transmit, or GPIO
CAN2RX	H1				CAN2 receive, or GPIO
CAN2TX	H2				CAN2 transmit, or GPIO
CAN3RX	M19				CAN3 receive, or GPIO
CAN3TX	M18				CAN3 transmit, or GPIO

4.1.1.1.6 Local Interconnect Network Interface Module (LIN)

Table 4-6. GWT Local Interconnect Network Interface Module (LIN)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
LINRX	A7	I/O	Pull Up	Programmable, 20uA	LIN receive, or GPIO
LINTX	B7				LIN transmit, or GPIO

4.1.1.1.7 Standard Serial Communication Interface (SCI)

Table 4-7. GWT Standard Serial Communication Interface (SCI)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
N2HET1[6]/**SCIRX**	W3	I/O	Pull Down	Programmable, 20uA	SCI receive, or GPIO
N2HET1[13]/**SCITX**	N2				SCI transmit, or GPIO

4.1.1.1.8 Inter-Integrated Circuit Interface Module (I2C)

Table 4-8. GWT Inter-Integrated Circuit Interface Module (I2C)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
MIBSPI3NCS[2]/**I2C_SDA**/N2HET1[27]	B2	I/O	Pull Up	Programmable, 20uA	I2C serial data, or GPIO
MIBSPI3NCS[3]/**I2C_SCL**/N2HET1[29]	C3				I2C serial clock, or GPIO

4.1.1.1.9 Standard Serial Peripheral Interface (SPI)

Table 4-9. GWT Standard Serial Peripheral Interface (SPI)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
SPI2CLK	E2	I/O	Pull Up	Programmable, 20uA	SPI2 clock, or GPIO
SPI2NCS[0]	N3				SPI2 chip select, or GPIO
SPI2NENA/**SPI2NCS[1]**	D3				SPI2 chip select, or GPIO
SPI2NENA/SPI2NCS[1]	D3				SPI2 enable, or GPIO
SPI2SIMO[0]	D1				SPI2 slave-input master-output, or GPIO
SPI2SOMI[0]	D2				SPI2 slave-output master-input, or GPIO
N2HET1[0]/**SPI4CLK**	K18	I/O	Pull Down	Programmable, 20uA	SPI4 clock, or GPIO
N2HET1[3]/**SPI4NCS[0]**/N2HET2[10]	U1				SPI4 chip select, or GPIO
N2HET1[1]/**SPI4NENA**/N2HET2[8]	V2				SPI4 enable, or GPIO
N2HET1[2]/**SPI4SIMO[0]**	W5				SPI4 slave-input master-output, or GPIO
N2HET1[5]/**SPI4SOMI[0]**/N2HET2[12]	V6				SPI4 slave-output master-input, or GPIO

4.1.1.1.10 Multi-Buffered Serial Peripheral Interface Modules (MibSPI)

Table 4-10. GWT Multi-Buffered Serial Peripheral Interface Modules (MibSPI)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
MIBSPI1CLK	F18	I/O	Pull Up	Programmable, 20uA	MibSPI1 clock, or GPIO
MIBSPI1NCS[0]/MIBSPI1SOMI[1]	R2				MibSPI1 chip select, or GPIO
MIBSPI1NCS[1]/N2HET1[17]	F3				
MIBSPI1NCS[2]/N2HET1[19]	G3				
MIBSPI1NCS[3]/N2HET1[21]	J3				
N2HET1[15]/**MIBSPI1NCS[4]**	N1		Pull Down	Programmable, 20uA	MibSPI1 chip select, or GPIO
N2HET1[24]/**MIBSPI1NCS[5]**	P1				
MIBSPI1NENA/N2HET1[23]	G19		Pull Up	Programmable, 20uA	MibSPI1 enable, or GPIO
MIBSPI1SIMO[0]	F19				MibSPI1 slave-in master-out, or GPIO
N2HET1[8]/**MIBSPI1SIMO[1]**	E18		Pull Down	Programmable, 20uA	MibSPI1 slave-in master-out, or GPIO
MIBSPI1SOMI[0]	G18		Pull Up	Programmable, 20uA	MibSPI1 slave-out master-in, or GPIO
MIBSPI1NCS[0]/**MIBSPI1SOMI[1]**	R2				
MIBSPI3CLK	V9	I/O	Pull Up	Programmable, 20uA	MibSPI3 clock, or GPIO
MIBSPI3NCS[0]/AD2EVT/GIOB[2]/N2HET2_PIN_nDIS	V10				MibSPI3 chip select, or GPIO
MIBSPI3NCS[1]/N2HET1[25]/MDCLK	V5				
MIBSPI3NCS[2]/I2C_SDA/N2HET1[27]	B2				
MIBSPI3NCS[3]/I2C_SCL/N2HET1[29]	C3				
N2HET1[11]/**MIBSPI3NCS[4]**/N2HET2[18]	E3		Pull Down	Programmable, 20uA	MibSPI3 chip select, or GPIO
MIBSPI3NENA/**MIBSPI3NCS[5]**/N2HET1[31]	W9		Pull Up	Programmable, 20uA	MibSPI3 chip select, or GPIO
MIBSPI3NENA/MIBSPI3NCS[5]/N2HET1[31]	W9				MibSPI3 enable, or GPIO
MIBSPI3SIMO[0]	W8				MibSPI3 slave-in master-out, or GPIO
MIBSPI3SOMI[0]	V8				MibSPI3 slave-out master-in, or GPIO
MIBSPI5CLK/DMM_DATA[4]	H19	I/O	Pull Up	Programmable, 20uA	MibSPI5 clock, or GPIO
MIBSPI5NCS[0]/DMM_DATA[5]	E19				MibSPI5 chip select, or GPIO
MIBSPI5NCS[1]/DMM_DATA[6]	B6				
MIBSPI5NCS[2]/DMM_DATA[2]	W6				
MIBSPI5NCS[3]/DMM_DATA[3]	T12				
MIBSPI5NENA/DMM_DATA[7]/	H18				MibSPI5 enable, or GPIO
MIBSPI5SIMO[0]/DMM_DATA[8]	J19				MibSPI5 slave-in master-out, or GPIO
MIBSPI5SIMO[1]/DMM_DATA[9]	E16				
MIBSPI5SIMO[2]/DMM_DATA[10]	H17				
MIBSPI5SIMO[3]/DMM_DATA[11]	G17				
MIBSPI5SOMI[0]/DMM_DATA[12]	J18				
MIBSPI5SOMI[1]/DMM_DATA[13]	E17				
MIBSPI5SOMI[2]/DMM_DATA[14]	H16				
MIBSPI5SOMI[3]/DMM_DATA[15]	G16				

4.1.1.1.11 Ethernet Controller

Table 4-11. GWT Ethernet Controller: MDIO Interface

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
MIBSPI3NCS[1]/N2HET1[25]/**MDCLK**	V5	Output	Pull Up	-	Serial clock output
MIBSPI1NCS[2]/N2HET1[19]/**MDIO**	G3	I/O	Pull Up	Fixed, 20uA	Serial data input/output

Table 4-12. GWT Ethernet Controller: Reduced Media Independent Interface (RMII)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
N2HET1[12]/MII_CRS/**RMII_CRS_DV**	B4	Input	Pull Down	Fixed, 20uA	RMII carrier sense and data valid
N2HET1[28]/MII_RX_CLK/**RMII_REFCLK**/MII_RX_AVCLK4	K19				RMII synchronous reference clock for receive, transmit and control interface
AD1EVT/MII_RX_ER/**RMII_RX_ER**	N19				RMII receive error
N2HET1[24]/MIBSPI1NCS[5]/MII_RXD[0]/**RMII_RXD[0]**	P1				RMII receive data
N2HET1[26]/MII_RXD[1]/**RMII_RXD[1]**	A14				
MIBSPI5SOMI[0]/DMM_DATA[12]/MII_TXD[0]/**RMII_TXD[0]**	J18	Output	Pull Up	-	RMII transmit data
MIBSPI5SIMO[0]/DMM_DATA[8]/MII_TXD[1]/**RMII_TXD[1]**	J19				
MIBSPI5CLK/DMM_DATA[4]/MII_TXEN/**RMII_TXEN**	H19				RMII transmit enable

Table 4-13. GWT Ethernet Controller: Media Independent Interface (MII)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
MIBSPI1NCS[1]/N2HET1[17]/**MII_COL**	F3	Input	Pull Up	-	Collision detect
N2HET1[12]/**MII_CRS**/RMII_CRS_DV	B4		Pull Down	Fixed, 20uA	Carrier sense and receive valid
N2HET1[28]/MII_RX_CLK/RMII_REFCLK/**MII_RX_AVCLK4**	K19	I/O	Pull Down	-	MII output receive clock
N2HET1[30]/**MII_RX_DV**	B11	Input	Pull Down	Fixed, 20uA	Received data valid
AD1EVT/**MII_RX_ER**/RMII_RX_ER	N19				Receive error
N2HET1[28]/**MII_RX_CLK**/RMII_REFCLK/MII_RX_AVCLK4	K19	I/O			Receive clock
N2HET1[24]/MIBSPI1NCS[5]/**MII_RXD[0]**/RMII_RXD[0]	P1	Input			Receive data
N2HET1[26]/**MII_RXD[1]**/RMII_RXD[1]	A14				
MIBSPI1NENA/N2HET1[23]/**MII_RXD[2]**	G19		Pull Up	Fixed, 20uA	
MIBSPI5NENA/DMM_DATA[7]/	H18				
N2HET1[10]/MII_TX_CLK/**MII_TX_AVCLK4**	D19	I/O	Pull Down	-	MII output transmit clock
N2HET1[10]/**MII_TX_CLK**/MII_TX_AVCLK4	D19				Transmit clock
MIBSPI5SOMI[0]/DMM_DATA[12]/RMII_TXD[0]	J18	Output	Pull Up	-	Transmit data
MIBSPI5SIMO[0]/DMM_DATA[8]/RMII_TXD[1]	J19				
MIBSPI1NCS[0]/MIBSPI1SOMI[1]/**MII_TXD[2]**	R2				
N2HET1[8]/MIBSPI1SIMO[1]/**MII_TXD[3]**	E18		Pull Down	-	
MIBSPI5CLK/DMM_DATA[4]/RMII_TXEN	H19		Pull Up	-	Transmit enable

4.1.1.1.12 External Memory Interface (EMIF)

Table 4-14. External Memory Interface (EMIF)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
EMIF_CKE	L3	Output	Pull Down	Programmable, 20uA	EMIF Clock Enablen
EMIF_CLK	K3	I/O			EMIF clock. This is an output signal in functional mode. It is gated off by default, so that the signal is tri-stated. PINMUX29[8] must be cleared to enable this output.
EMIF_nWE/**EMIF_RNW**	D17	Output	Pull Up	Programmable, 20uA	EMIF Read-Not-Write
ETMDATA[13]/**EMIF_nOE**	E12		Pull Down	Programmable, 20uA	EMIF Output Enable
EMIF_nWAIT	P3	I/O	Pull Up	Fixed, 20uA	EMIF Extended Wait Signal
EMIF_nWE/EMIF_RNW	D17	Output	Pull Up	Programmable, 20uA	EMIF Write Enable.
EMIF_nCAS	R4	Output			EMIF column address strobe
EMIF_nRAS	R3	Output			EMIF row address strobe
EMIF_nCS[0]/RTP_DATA[15]/N2HET2[7]	N17	Output	Pull Down	Programmable, 20uA	EMIF chip select, SDRAM
EMIF_nCS[2]	L17	Output	Pull Up	Programmable, 20uA	EMIF chip selects, asynchronous This applies to chip selects 2, 3 and 4
EMIF_nCS[3]/RTP_DATA[14]/N2HET2[9]	K17	Output	Pull Down	Programmable, 20uA	
EMIF_nCS[4]/RTP_DATA[7]	M17	Output	Pull Up	Programmable, 20uA	

Table 4-14. External Memory Interface (EMIF) (continued)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
ETMDATA[15]/**EMIF_nDQM[0]**	E10	Output	Pull Down	Programmable, 20uA	EMIF Data Mask or Write Strobe. Data mask for SDRAM devices, write strobe for connected asynchronous devices.
ETMDATA[14]/**EMIF_nDQM[1]**	E11	Output			
ETMDATA[12]/**EMIF_BA[0]**	E13	Output			EMIF bank address or address line
EMIF_BA[1]/N2HET2[5]	D16	Output			EMIF bank address or address line
EMIF_ADDR[0]/N2HET2[1]	D4	Output			EMIF address
EMIF_ADDR[1]/N2HET2[3]	D5	Output			
ETMDATA[11]/**EMIF_ADDR[2]**	E6	Output			
ETMDATA[10]/**EMIF_ADDR[3]**	E7	Output			
ETMDATA[9]/**EMIF_ADDR[4**	E8	Output			
ETMDATA[8]/**EMIF_ADDR[5]**	E9	Output			
EMIF_ADDR[6]/RTP_DATA[13]	C4	Output			
EMIF_ADDR[7]/RTP_DATA[12]	C5	Output			
EMIF_ADDR[8]/RTP_DATA[11]	C6	Output			
EMIF_ADDR[9]/RTP_DATA[10]	C7	Output			
EMIF_ADDR[10]/RTP_DATA[9]	C8	Output			
EMIF_ADDR[11]/RTP_DATA[8]	C9	Output			
EMIF_ADDR[12]/RTP_DATA[6]	C10	Output			
EMIF_ADDR[13]/RTP_DATA[5]	C11	Output			
EMIF_ADDR[14]/RTP_DATA[4]	C12	Output			
EMIF_ADDR[15]/RTP_DATA[3]	C13	Output			
EMIF_ADDR[16]/RTP_DATA[2]	D14	Output			
EMIF_ADDR[17]/RTP_DATA[1]	C14	Output	Pull Down	-	
EMIF_ADDR[18]/RTP_DATA[0]	D15	Output			
EMIF_ADDR[19]/RTP_nENA	C15	Output			
EMIF_ADDR[20]/RTP_nSYNC	C16	Output			
EMIF_ADDR[21]/RTP_CLK	C17	Output			
ETMDATA[16]/**EMIF_DATA[0]**	K15	I/O	Pull Down	Fixed, 20uA	EMIF Data
ETMDATA[17]/**EMIF_DATA[1]**	L15	I/O			
ETMDATA[18]/**EMIF_DATA[2]**	M15	I/O			
ETMDATA[19]/**EMIF_DATA[3]**	N15	I/O			
ETMDATA[20]/**EMIF_DATA[4]**	E5	I/O			
ETMDATA[21]/**EMIF_DATA[5]**	F5	I/O			
ETMDATA[22]/**EMIF_DATA[6]**	G5	I/O			
ETMDATA[23]/**EMIF_DATA[7]**	K5	I/O			
ETMDATA[24]/**EMIF_DATA[8]**	L5	I/O			
ETMDATA[25]/**EMIF_DATA[9]**	M5	I/O			
ETMDATA[26]/**EMIF_DATA[10]**	N5	I/O			
ETMDATA[27]/**EMIF_DATA[11]**	P5	I/O			
ETMDATA[28]/**EMIF_DATA[12]**	R5	I/O			
ETMDATA[29]/**EMIF_DATA[13]**	R6	I/O			
ETMDATA[30]/**EMIF_DATA[14]**	R7	I/O			
ETMDATA[31]/**EMIF_DATA[15]**	R8	I/O			

4.1.1.1.13 Embedded Trace Macrocell for Cortex-R4F CPU (ETM-R4F)

Table 4-15. Embedded Trace Macrocell for Cortex-R4F CPU (ETM-R4F)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
ETMTRACECLKIN/EXTCLKIN2	R9	Input	Pull Down	Fixed, 20uA	ETM Trace Clock Input
ETMTRACECLKOUT	R10	Output	Pull Down	-	ETM Trace Clock Output
ETMTRACECTL	R11	Output	Pull Down	-	ETM trace control
ETMDATA[0]	R12				ETM data
ETMDATA[1]	R13				
ETMDATA[2]	J15				
ETMDATA[3]	H15				
ETMDATA[4]	G15				
ETMDATA[5]	F15				
ETMDATA[6]	E15				
ETMDATA[7]	E14				
ETMDATA[8]/EMIF_ADDR[5]	E9				
ETMDATA[9]/EMIF_ADDR[4]	E8				
ETMDATA[10]/EMIF_ADDR[3]	E7				
ETMDATA[11]/EMIF_ADDR[2]	E6				
ETMDATA[12]/EMIF_BA[0]	E13				
ETMDATA[13]/EMIF_nOE	E12				
ETMDATA[14]/EMIF_nDQM[1]	E11				
ETMDATA[15]/EMIF_nDQM[0]	E10				
ETMDATA[16]/EMIF_DATA[0]	K15				
ETMDATA[17]/EMIF_DATA[1]	L15				
ETMDATA[18]/EMIF_DATA[2]	M15				
ETMDATA[19]/EMIF_DATA[3]	N15				
ETMDATA[20]/EMIF_DATA[4]	E5				
ETMDATA[21]/EMIF_DATA[5]	F5				
ETMDATA[22]/EMIF_DATA[6]	G5				
ETMDATA[23]/EMIF_DATA[7]	K5				
ETMDATA[24]/EMIF_DATA[8]	L5				
ETMDATA[25]/EMIF_DATA[9]	M5				
ETMDATA[26]/EMIF_DATA[10]	N5				
ETMDATA[27]/EMIF_DATA[11]	P5				
ETMDATA[28]/EMIF_DATA[12]	R5				
ETMDATA[29]/EMIF_DATA[13]	R6				
ETMDATA[30]/EMIF_DATA[14]	R7				
ETMDATA[31]/EMIF_DATA[15]	R8				

4.1.1.1.14 RAM Trace Port (RTP)

Table 4-16. RAM Trace Port (RTP)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
EMIF_ADDR[21]/**RTP_CLK**	C17	I/O	Pull Down	Programmable, 20uA	RTP packet clock, or GPIO
EMIF_ADDR[19]/**RTP_nENA**	C15	I/O			RTP packet handshake, or GPIO
EMIF_ADDR[20]/**RTP_nSYNC**	C16	I/O			RTP synchronization, or GPIO
EMIF_ADDR[18]/**RTP_DATA[0]**	D15	I/O			RTP packet data, or GPIO
EMIF_ADDR[17]/**RTP_DATA[1]**	C14				
EMIF_ADDR[16]/**RTP_DATA[2]**	D14				
EMIF_ADDR[15]/**RTP_DATA[3]**	C13				
EMIF_ADDR[14]/**RTP_DATA[4]**	C12				
EMIF_ADDR[13]/**RTP_DATA[5]**	C11				
EMIF_ADDR[12]/**RTP_DATA[6]**	C10				
EMIF_nCS[4]/**RTP_DATA[7]**	M17		Pull Up	Programmable, 20uA	
EMIF_ADDR[11]/**RTP_DATA[8]**	C9		Pull Down	Programmable, 20uA	
EMIF_ADDR[10]/**RTP_DATA[9]**	C8				
EMIF_ADDR[9]/**RTP_DATA[10]**	C7				
EMIF_ADDR[8]/**RTP_DATA[11]**	C6				
EMIF_ADDR[7]/**RTP_DATA[12]**	C5				
EMIF_ADDR[6]/**RTP_DATA[13]**	C4				
EMIF_nCS[0]/**RTP_DATA[15]**/N2HET2[7]	N17				
EMIF_nCS[3]/**RTP_DATA[14]**/N2HET2[9]	K17				

4.1.1.1.15 Data Modification Module (DMM)

Table 4-17. Data Modification Module (DMM)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
DMM_CLK	F17	I/O	Pull Up	Programmable, 20uA	DMM clock, or GPIO
DMM_nENA	F16				DMM handshake, or GPIO
DMM_SYNC	J16				DMM synchronization, or GPIO
DMM_DATA[0]	L19				DMM data, or GPIO
DMM_DATA[1]	L18				
MIBSPI5NCS[2]/**DMM_DATA[2]**	W6				
MIBSPI5NCS[3]/**DMM_DATA[3]**	T12				
MIBSPI5CLK/**DMM_DATA[4]**	H19				
MIBSPI5NCS[0]/**DMM_DATA[5]**	E19				
MIBSPI5NCS[1]/**DMM_DATA[6]**	B6				
MIBSPI5NENA/**DMM_DATA[7]**	H18				
MIBSPI5SIMO[0]/**DMM_DATA[8]**	J19				
MIBSPI5SIMO[1]/**DMM_DATA[9]**	E16				
MIBSPI5SIMO[2]/**DMM_DATA[10]**	H17				
MIBSPI5SIMO[3]/**DMM_DATA[11]**	G17				
MIBSPI5SOMI[0]/**DMM_DATA[12]**	J18				
MIBSPI5SOMI[1]/**DMM_DATA[13]**	E17				
MIBSPI5SOMI[2]/**DMM_DATA[14]**	H16				
MIBSPI5SOMI[3]/**DMM_DATA[15]**	G16				

4.1.1.1.16 System Module Interface

Table 4-18. GWT System Module Interface

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
nPORRST	W7	Input	Pull Down	100uA	Power-on reset, cold reset External power supply monitor circuitry must drive nPORRST low when any of the supplies to the microcontroller fall out of the specified range. This terminal has a glitch filter. See Section 6.8.
nRST	B17	I/O	Pull Up	100uA	System reset, warm reset, bidirectional. The internal circuitry indicates any reset condition by driving nRST low. The external circuitry can assert a system reset by driving nRST low. To ensure that an external reset is not arbitrarily generated, TI recommends that an external pull-up resistor is connected to this terminal. This terminal has a glitch filter. See Section 6.8.
nERROR	B14	I/O	Pull Down	20uA	ESM Error Signal Indicates error of high severity. See Section 6.18.

4.1.1.1.17 Clock Inputs and Outputs

Table 4-19. GWT Clock Inputs and Outputs

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
OSCIN	K1	Input	-	-	From external crystal/resonator, or external clock input
KELVIN_GND	L2	Input			Kelvin ground for oscillator
OSCOUT	L1	Output			To external crystal/resonator
ECLK	A12	I/O	Pull Down	Programmable, 20uA	External prescaled clock output, or GIO.
GIOA[5]/**EXTCLKIN**/N2HET1_PIN_nDIS	B5	Input	Pull Down	20uA	External clock input #1
ETMTRACECLKIN/**EXTCLKIN2**	R9	Input			External clock input #2
VCCPLL	P11	1.2V Power		-	Dedicated core supply for PLL's

4.1.1.1.18 Test and Debug Modules Interface

Table 4-20. GWT Test and Debug Modules Interface

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
TEST	U2	I/O	Pull Down	Fixed, 100uA	Test enable
nTRST	D18	Input			JTAG test hardware reset
RTCK	A16	Output	-	None	JTAG return test clock
TCK	B18	Input	Pull Down	Fixed, 100uA	JTAG test clock
TDI	A17	I/O	Pull Up		JTAG test data in
TDO	C18	I/O	Pull Down		JTAG test data out
TMS	C19	I/O	Pull Up		JTAG test select

4.1.1.1.19 Flash Supply and Test Pads

Table 4-21. GWT Flash Supply and Test Pads

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
VCCP	F8	3.3V Power	-	None	Flash pump supply
FLTP1	J5				Flash test pads. These terminals are reserved for TI use only. For proper operation these terminals must connect only to a test pad or not be connected at all [no connect (NC)].
FLTP2	H5				

4.1.1.1.20 No Connects

Table 4-22. No Connects

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
NC	A8	-	-	-	No Connects. These balls are not connected to any internal logic and can be connected to the PCB ground without affecting the functionality of the device. Any other ball marked as "NC" may be internally connected to some functionality. It is recommended for such balls to be left unconnected.
NC	B8	-	-	-	
NC	B9	-	-	-	
NC	D6	-	-	-	
NC	D7	-	-	-	
NC	D8	-	-	-	
NC	D9	-	-	-	
NC	D10	-	-	-	
NC	D11	-	-	-	
NC	D12	-	-	-	
NC	D13	-	-	-	
NC	E4	-	-	-	
NC	F4	-	-	-	
NC	G4	-	-	-	
NC	K4	-	-	-	
NC	K16	-	-	-	
NC	L4	-	-	-	
NC	L16	-	-	-	
NC	M4	-	-	-	
NC	M16	-	-	-	
NC	N4	-	-	-	
NC	N16	-	-	-	
NC	N18	-	-	-	
NC	P4	-	-	-	
NC	P15	-	-	-	
NC	P16	-	-	-	
NC	P17	-	-	-	
NC	R1	-	-	-	
NC	R14	-	-	-	
NC	R15	-	-	-	
NC	T3	-	-	-	
NC	T4	-	-	-	
NC	T5	-	-	-	
NC	T6	-	-	-	
NC	T7	-	-	-	
NC	T8	-	-	-	
NC	T9	-	-	-	
NC	T10	-	-	-	
NC	T11	-	-	-	
NC	T13	-	-	-	
NC	T14	-	-	-	
NC	U3	-	-	-	
NC	U4	-	-	-	

Table 4-22. No Connects (continued)

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
NC	U6	-	-	-	No Connects. These balls are not connected to any internal logic and can be connected to the PCB ground without affecting the functionality of the device. Any other ball marked as "NC" may be internally connected to some functionality. It is recommended for such balls to be left unconnected.
NC	U7	-	-	-	
NC	U8	-	-	-	
NC	U9	-	-	-	
NC	U10	-	-	-	
NC	U11	-	-	-	
NC	V3	-	-	-	
NC	V4	-	-	-	
NC	V11	-	-	-	
NC	V12	-	-	-	
NC	W4	-	-	-	
NC	W11	-	-	-	
NC	W12	-	-	-	
NC	W13	-	-	-	

4.1.1.1.21 Supply for Core Logic: 1.2V nominal

Table 4-23. GWT Supply for Core Logic: 1.2V nominal

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
VCC	F9	1.2V Power	-	None	Core supply
VCC	F10				
VCC	H10				
VCC	J14				
VCC	K6				
VCC	K8				
VCC	K12				
VCC	K14				
VCC	L6				
VCC	M10				
VCC	P10				

4.1.1.1.22 Supply for I/O Cells: 3.3V nominal

Table 4-24. GWT Supply for I/O Cells: 3.3V nominal

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
VCCIO	F6	3.3V Power	-	None	Operating supply for I/Os
VCCIO	F7				
VCCIO	F11				
VCCIO	F12				
VCCIO	F13				
VCCIO	F14				
VCCIO	G6				
VCCIO	G14				
VCCIO	H6				
VCCIO	H14				
VCCIO	J6				
VCCIO	L14				
VCCIO	M6				
VCCIO	M14				
VCCIO	N6				
VCCIO	N14				
VCCIO	P6				
VCCIO	P7				
VCCIO	P8				
VCCIO	P9				
VCCIO	P12				
VCCIO	P13				
VCCIO	P14				

4.1.1.1.23 Ground Reference for All Supplies Except VCCAD

Table 4-25. GWT Ground Reference for All Supplies Except VCCAD

Pin		Signal Type	Default Pull State	Pull Type	Description
Signal Name	337 GWT				
VSS	A1	Ground	-	None	Ground reference
VSS	A2				
VSS	A18				
VSS	A19				
VSS	B1				
VSS	B19				
VSS	H8				
VSS	H9				
VSS	H11				
VSS	H12				
VSS	J8				
VSS	J9				
VSS	J10				
VSS	J11				
VSS	J12				
VSS	K9				
VSS	K10				
VSS	K11				
VSS	L8				
VSS	L9				
VSS	L10				
VSS	L11				
VSS	L12				
VSS	M8				
VSS	M9				
VSS	M11				
VSS	M12				
VSS	V1				
VSS	W1				
VSS	W2				